AMENDMENTS TO THE CLAIMS

Please amend the claims as follows.

1. (Currently Amended) A semiconductor tester, comprising:

a driver circuit for supplying a signal of a predetermined waveform to be applied to an IC pin of a device under test (DUT) via a predetermined transmission line, wherein said driver circuit comprises:

means for receiving a driver input pulse of a logic signal, detecting a rising edge of said driver input pulse and generating a differential rise correction pulse to perform a peaking correction on a rise of a waveform;

means for receiving a driver input pulse of a logic signal, detecting a falling edge of said driver input pulse and generating a differential fall correction pulse to perform a peaking correction on a fall of a waveform; and

means for performing said peaking correction on a rising part of a waveform outputted from said driver circuit based on said differential rise correction pulse, ~~whereas~~ while performing a peaking correction on a falling part of a waveform outputted from said driver circuit based on said differential fall correction pulse.

2. (Currently Amended) A semiconductor tester, comprising:

a driver circuit for supplying a signal of a predetermined waveform to be applied to an IC pin of a device under test (DUT) via a predetermined transmission line,

wherein said driver circuit comprises:

drive pulse generating means for receiving a rising edge of a driver input pulse of a logic signal and generating a differential rise correction pulse, ~~whereas~~ while receiving a falling edge of a driver input pulse of a logic signal and generating a differential fall correction pulse;

a rise pulse superimposing section for receiving said differential rise correction pulse and generating a first sink current whose current amount corresponds to said differential rose correction pulse;

a fall pulse superimposing section for receiving said fall correction pulse and generating a second sink current whose current amount corresponds to said fall correction pulse; and

preceding and last stages of said driver circuit for outputting a test waveform to be supplied to said DUT by receiving said first sink current and performing a peaking correction on a rising side of said test waveform, while receiving said second sink current and performing a peaking correction on a falling side of said test waveform.

3. (Currently Amended) A semiconductor tester, comprising:

a driver circuit for supplying a signal of a predetermined waveform to be applied to an IC pin of a device under test (DUT) via a predetermined transmission line,

wherein said driver circuit comprises:

a plurality (n) of drive pulse generating means, each of which receives a rising edge of a driver input pulse of a logic signal and generates a differential rise correction pulse so that said rise correction pulse has a different pulse period, ~~whereas~~ while receiving a falling edge of a driver input pulse of a logic signal and generating a differential fall correction pulse so that said fall correction pulse has a different pulse period;

a plurality (n) of rise pulse superimposing sections, each of which receives a plurality (n) of said differential rise correction pulses and generates a first sink current of a predetermined sink current amount for a predetermined pulse period;

a plurality (n) of fall pulse superimposing sections, each of which receives a plurality (n) of said fall correction pulses and generates a second sink current of a predetermined sink current amount for a predetermined pulse period; and

preceding and last stages of said driver circuit for outputting a test waveform to be supplied to said DUT by receiving a plurality (n) of said first sink currents and performing a peaking correction on a rising side of said test waveform, while receiving a plurality (n) of said second sink currents and performing a peaking correction on a falling side of said test waveform.

4. (Currently Amended) A semiconductor tester as claimed in claim 2 [[or 3]],

wherein said drive pulse generating means receives a drive input pulse of a logic signal,

firstly detects a rising edge of said driver input pulse and generates a differential rise correction pulse of a predetermined period,

secondly detects a falling edge of said driver input pulse and generates a differential fall correction pulse of a predetermined period, and

thirdly generates a differential driver pulse corresponding to said driver input pulse.

5. (Currently Amended) A semiconductor tester as claimed in claim 2 [[or 3]],

wherein said rise pulse superimposing section comprises a first constant current source and first and second transistors of a first differential amplification configuration,

said first constant current source is coupled to emitters of ~~said~~ both of said transistors and makes a constant current amount flowing through any of ~~said~~ both of said transistors be constant, and

said first and second transistors receive said differential rise correction pulse in base terminals thereof and generate a first sink current of a constant current amount on which current switching has been performed.

6. (Currently Amended) A semiconductor tester as claimed in claim 2 [[or 3]],

wherein said fall pulse superimposing section comprises a second constant current source and third and fourth transistors of a second differential amplification configuration,

said second constant current source is coupled to emitters of ~~said~~ both of said transistors and makes a constant current amount flowing through any of ~~said~~ both of said transistors be constant, and

said third and fourth transistors receive said differential rise correction pulse in base terminals thereof and generate a second sink current of a constant current amount on which current switching has been performed.

7. (Currently Amended) A semiconductor tester as claimed in claim 2 [[or 3]],

wherein said preceding stage of said driver circuit, which supplies a differential drive voltage signal to determine a voltage level, which is a high or low level, to be outputted from said last stage, comprises first and second resistors, a third constant current source, and fifth and sixth transistors of a third differential amplification configuration,

said first resistor, which is a load resistor coupled to a collector of said fifth transistor, is coupled to a collector terminal of ~~said~~ a first transistor for generating said first sink current of said rise pulse superimposing section,

said second resistor, which is a load resistor coupled to a collector of said sixth transistor, is coupled to a collector terminal of ~~said~~ a third transistor for generating said second sink current of said fall pulse superimposing section,

said third constant current source is coupled to both emitters of said third differential transistors and allows a predetermined constant current amount to flow, and

current switching is preformed based on a differential drive pulse received by ~~said~~ both of said transistors of said third differential amplification configuration, while said differential drive voltage signal weighted by said first and second sink currents is outputted from collectors of ~~said~~ both of said transistors and supplied to said last stage.

8. (Currently Amended) A semiconductor tester as claimed in claim 2 [[or 3]],

wherein said last stage of said driver circuit comprises seventh and eighth transistors of a fourth differential amplification configuration, first and second current dividing resistors, a first load resistor, and a fourth constant current source,

said seventh and eighth transistors receive said differential drive voltage signal outputted from said preceding stage of said driver circuit in a base input terminal thereof, amplify said differential drive voltage signal in a predetermined manner, and generate an applied signal of a predetermined waveform to be supplied to said DUT from a collector terminal of said eighth transistor,

said first and second current dividing resistors, which are emitter resistors individually coupled to emitters of ~~said~~ both of said transistors, while other ends of said current dividing resistors are coupled to said fourth constant current source,

said first load resistor, which becomes a load resistor coupled to said constant current source and said collector terminal of said eighth transistor, supplies said applied signal of a predetermined waveform to said DUT, and

said fourth constant current source becomes a constant current source inserted between a negative power source and said first and second current dividing resistors.

9. (Currently Amended) A semiconductor tester as claimed in claim 5 [[or 6]],

wherein said first or second constant current source is a fixed constant current source for supplying an invariable constant current amount or a variable constant current source whose constant current amount is externally changeable.

10. (New) A semiconductor tester as claimed in claim 3,

wherein said drive pulse generating means receives a drive input pulse of a logic signal,

firstly detects a rising edge of said driver input pulse and generates a differential rise correction pulse of a predetermined period,

secondly detects a falling edge of said driver input pulse and generates a differential fall correction pulse of a predetermined period, and

thirdly generates a differential driver pulse corresponding to said driver input pulse.

11. (New) A semiconductor tester as claimed in claim 3,

wherein said rise pulse superimposing section comprises a first constant current source and first and second transistors of a first differential amplification configuration,

said first constant current source is coupled to emitters of said both of said transistors and makes a constant current amount flowing through any of said both of said transistors be constant, and

said first and second transistors receive said differential rise correction pulse in base terminals thereof and generate a first sink current of a constant current amount on which current switching has been performed.

12. (New) A semiconductor tester as claimed in claim 3,

wherein said fall pulse superimposing section comprises a second constant current source and third and fourth transistors of a second differential amplification configuration,

said second constant current source is coupled to emitters of said both of said transistors and makes a constant current amount flowing through any of said both of said transistors be constant, and

said third and fourth transistors receive said differential rise correction pulse in base terminals thereof and generate a second sink current of a constant current amount on which current switching has been performed.

13. (New) A semiconductor tester as claimed in claim 3,

wherein said preceding stage of said driver circuit, which supplies a differential drive voltage signal to determine a voltage level, which is a high or low level, to be outputted from said last stage, comprises first and second resistors, a third constant current source, and fifth and sixth transistors of a third differential amplification configuration,

said first resistor, which is a load resistor coupled to a collector of said fifth transistor, is coupled to a collector terminal of said a first transistor for generating said first sink current of said rise pulse superimposing section,

said second resistor, which is a load resistor coupled to a collector of said sixth transistor, is coupled to a collector terminal of said a third transistor for generating said second sink current of said fall pulse superimposing section,

said third constant current source is coupled to both emitters of said third differential transistors and allows a predetermined constant current amount to flow, and

current switching is preformed based on a differential drive pulse received by said both of said transistors of said third differential amplification configuration, while said differential drive voltage signal weighted by said first and second sink currents is outputted from collectors of said both of said transistors and supplied to said last stage.

14. (New) A semiconductor tester as claimed in claim 3,

wherein said last stage of said driver circuit comprises seventh and eighth transistors of a fourth differential amplification configuration, first and second current dividing resistors, a first load resistor, and a fourth constant current source,

said seventh and eighth transistors receive said differential drive voltage signal outputted from said preceding stage of said driver circuit in a base input terminal thereof, amplify said differential drive voltage signal in a predetermined manner, and generate an applied signal of a

predetermined waveform to be supplied to said DUT from a collector terminal of said eighth transistor,

said first and second current dividing resistors, which are emitter resistors individually coupled to emitters of said both of said transistors, while other ends of said current dividing resistors are coupled to said fourth constant current source,

said first load resistor, which becomes a load resistor coupled to said constant current source and said collector terminal of said eighth transistor, supplies said applied signal of a predetermined waveform to said DUT, and

said fourth constant current source becomes a constant current source inserted between a negative power source and said first and second current dividing resistors.

15. (New) A semiconductor tester as claimed in claim 6,

wherein said first or second constant current source is a fixed constant current source for supplying an invariable constant current amount or a variable constant current source whose constant current amount is externally changeable.